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Applicant : **MITSUBISHI DENKI KABUSHIKI  
KAISHA**  
2-3, Marunouchi 2-chome Chiyoda-ku  
Tokyo (JP)

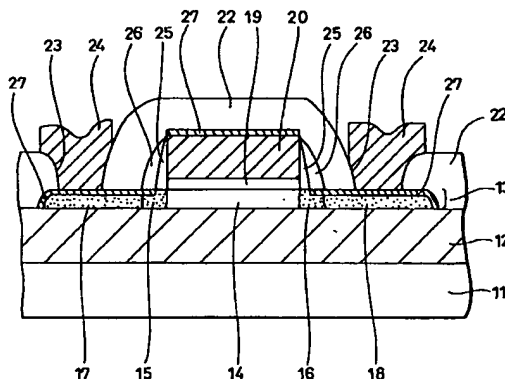
Inventor : Yamaguchi, Yasuo, c/o Mitsubishi  
Denki K.K.  
LSI Kenkyusho, 1 Mizuhara 4-chome  
Itami-shi, Hyogo-ken (JP)  
Inventor : Ajika, Natsuo, c/o Mitsubishi Denki  
K.K.  
LSI Kenkyusho, 1 Mizuhara 4-chome  
Itami-shi, Hyogo-ken (JP)  
Inventor : Yamano, Tsuyoshi, c/o Mitsubishi  
Denki K.K.  
LSI Kenkyusho, 1 Mizuhara 4-chome  
Itami-shi, Hyogo-ken (JP)

Representative : Beresford, Keith Denis Lewis  
et al  
**BERESFORD & Co.** 2-5 Warwick Court High  
Holborn  
London WC1R 5DJ (GB)

**Thin film transistor and a method of manufacturing thereof.**

A semiconductor device of a field effect transistor having an SOI structure is formed as below. Using a gate electrode 20 as a mask, n type impurities are implanted into an SOI layer (13) of p type to form additional source/drain regions (15, 16) of intermediate concentration. Then, a relatively thin sidewall spacer (25) is formed at the sidewall of the gate electrode (20). Using the sidewall spacer (25) as a mask, a titanium silicide layer (27) is formed in self-alignment on the surface of the SOI layer (13). Next, a relatively thick sidewall spacer (26) is formed. Using this sidewall spacer as a mask, n type impurities are implanted to form a source/drain region (17, 18) of high concentration. According to this manufacturing step, over-etching of the source/drain region (17, 18) are prevented in performing anisotropic etching at the time of sidewall spacer (25, 26) formation.

FIG. 5



## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to semiconductor devices, and more particularly, to a semiconductor device having a relatively thin active region such as a MOS (Metal Oxide Semiconductor) type field effect transistor (referred to as SOI-MOSFET hereinafter) and a method of manufacturing thereof.

### Description of the Background Art

An SOI-MOSFET to which the present invention is mainly applied will be explained first taking a complementary type MOS (referred to as CMOS hereinafter) as an example of the background technology of the present invention.

A CMOS having low consumption power and superior noise immunity is important in seeking high integration density and high speed operation. A sectional view of a conventional CMOS of not the SOI type but the so-called bulk type is shown in Fig. 1A. Referring to Fig. 1A, a CMOS has an n well region 2 formed in the proximity of the surface of a p type silicon substrate 1. A p channel type MOSFET 4 comprising a polycrystalline silicon gate 4 as the main element is formed on n well region 2. An n channel type MOSFET 6 comprising a polycrystalline silicon gate 5 as the main element is formed at the surface of p type silicon substrate 1 in the region other than n well region 2. A field oxide film 7 insulates and isolates n well region 2 from the other region. When such a bulk type CMOS is reduced in element size, parasitic thyristor is activated by noise from outside so that abnormal current flows from the power supply terminal to the ground terminal to stop the circuit operation (latch up phenomenon). This also induces problems such as soft error by  $\alpha$ -particle.

A sectional view of a CMOS having an SOI type structure is schematically shown in Fig. 1B. Referring to Fig. 1B, this SOI type CMOS has semiconductor layers 9 and 10 such as of silicon layers formed island-like by a field insulating film 7 on a silicon substrate 1 with an insulator layer 8 therebetween. Semiconductor layer 9 has an n type channel region and p type source/drain regions of p channel MOSFET 4 formed including polycrystalline silicon gate 3. Semiconductor layer 10 has a p type channel region and n type source/drain regions of n channel MOSFET 6 formed. Such a CMOS of the SOI structure has each element and also the substrate insulation-separated so that there is no current path leading to soft error and latch up. This is advantageous to reduction of element size. It is also advantageous to high speed operation since interconnection capacitance and junction capacitance are reduced by the lower insulating layer (refer to Ouyou Butsuri (Applied Physics)

Vol. 54, N. 12 (1985) pp. 1274 - 1283, "SOI Technology").

A structure of a conventional SOI-MOSFET and a method of manufacturing thereof will be explained hereinafter with reference to Figs. 2, and 3A - 3F. Referring to Fig. 2, a conventional SOI-MOSFET has an insulator layer 12 formed on a silicon substrate 11. A relatively thin silicon layer 13 of approximately 300 - 1500Å is formed on insulator layer 12. Near the center of silicon layer 13, a channel region 14 having a low p type impurity concentration (for example,  $10^{16}$  -  $10^{17}/\text{cm}^3$ ) is formed. An additional source region 15 and an additional drain region 16 having an n type impurity concentration of the middle degree (for example,  $10^{18}/\text{cm}^3$ ) are formed adjacent to the sides of channel region 14.

Additional source region 15 and additional drain region 16 have a source region 17 and a drain region 18 connected, respectively, each of a high n type impurity concentration (for example  $10^{19}$  -  $10^{20}/\text{cm}^3$ ).

A gate electrode 20 is formed above channel region 14 with a dielectric thin film 19 therebetween. A sidewall spacer 21 is formed at the sidewalls of gate electrode 20. Silicon layer 13, gate electrode 20 and sidewall spacer 21 are covered with an interlayer insulating film 22. A contact hole 23 is provided in interlayer insulating film 22. An interconnection layer 24 is connected to gate electrode 20, source region 17 and drain region 18 through each contact hole 23.

When positive voltage is applied to gate electrode 20 in the SOI-MOSFET of the above structure, carriers (electrons) of the n conductivity type are induced towards the upper layer of p type channel region 14, whereby that upper layer is inverted to an n conductivity type identical to the conductivity of source region 17 and drain region 18, or additional source region 15 and additional drain region 16. This allows current to flow between source region 17 and drain region 18. Because the concentration of the n type carriers induced at the upper layer of channel region 14 varies depending on the gate voltage, the current amount flowing across channel region 14 can be controlled by the gate voltage. This explains the operation of a MOSFET.

Additional drain region 16 has the so-called LDD (Lightly-Doped Drain) structure, serving to reduce the electric field in the proximity of the boundary between drain region 18 and gate electrode 20 to suppress generation of electron-hole pairs caused by impact ionization phenomenon. A thin film SOI-MOSFET having a relatively thin silicon layer 13 of, for example, 500 - 1500Å thickness, has the following characteristics in comparison with a conventional SOI-MOSFET having a relatively thick silicon layer of approximately 5000Å. Since channel region 14 where current flows is very thin, the application of a gate voltage causes channel region 14 to become entirely depleted. This allows the depletion layer of channel

region 14 to be controlled reliably by gate electrode 20 independent of the effect of the drain voltage. This reduces the effect of electric field from drain region 18 to channel region 14. As a result, the  $V_D-I_D$  characteristic degradation of Fig. 4A seen in conventional bulk type MOSFETs excluding the SOI type where current increases suddenly by a high drain voltage, i.e. the punch through phenomenon, is suppressed. It will therefore be possible to operate stably a transistor having a short gate length.

A method of manufacturing a conventional SOI-MOSFET having the structure of Fig. 2 will be explained hereinafter with reference to Figs. 3A - 3F. First, oxygen ions are implanted into a silicon substrate 11 at an injection energy of 200KeV and a dosage of  $2 \times 10^{19}/\text{cm}^2$ . Then, the substrate is subjected to heat treatment of approximately 1350°C. An insulating layer 12 is formed in silicon substrate 11 leaving a thin silicon layer 13 on the surface. Next, silicon layer 13 is processed in an island-like manner to form an active region (Fig. 3A). Impurities of p type are injected into silicon layer 13 to form a channel region 14. Next, a dielectric thin film 19 is formed by thermal oxidation of the surface of silicon layer 13. Then, a gate electrode 20 such as of polycrystalline silicon is formed. Ion implantation is carried out using gate electrode 20 as a mask. By implanting phosphorus which is an impurity of n type for example, additional source region 15 and additional drain region 16 are formed (Fig. 3B).

By depositing a CVD insulating film 21a (Fig. 3C) and then carrying out reactive ion etching, a sidewall spacer 21 is formed at the sidewall of gate electrode 20. Some over-etching is necessary in providing sidewall spacer 21. This is to take into consideration unevenness in the thickness of CVD oxide film 21a which is deposited to approximately 3000Å to leave only sidewall spacer 21 while removing the remainder by etching. This over-etching is responsible for some removal of silicon layer 13 to generate a step as shown in Fig. 3B by arrow A. Specifically, when the application of reactive ion etching to CVD oxide film 21a of, for example, approximately 3000Å in average is carried out with over-etching of approximately 20% on account of variation in thickness and etching characteristic of CVD oxide film 21a. That is to say, 3000Å of CVD oxide film 21a is first etched, followed by etching of a time period where 600Å of CVD oxide film 21a is over-etched. Silicon layer 13 will be over-etched if the thickness of the CVD insulating film deposited thereabove is exactly 3000Å. A silicon oxide film is generally used for a CVD insulating film, where the selectivity of reactive ion etching to silicon is approximately 5 : 1. This means that silicon of approximately 120Å is etched during the time period where over-etching of 600Å is carried out for a silicon oxide film.

Following the formation of sidewall spacer 21,

arsenic ions of  $10^{19} - 10^{20}/\text{cm}^3$  are injected using sidewall spacer 21 as a mask to form source region 17 and drain region 18 of high concentration, as shown in Fig. 3D. Then, an interlayer insulating film 22 is deposited by CVD, followed by formation of a contact hole 23 in a predetermined position in interlayer insulating layer 22. Some over-etching occurs in forming contact hole 23 to result in a depression indicated by arrow B in Fig. 3E. The formation of an interconnection layer 24 completes the manufacture of a thin film SOI-MOSFET of Fig. 3F.

Because a conventional SOI-MOSFET is manufactured having a structure as described above, over-etching occurs in forming sidewall spacer 21 and contact hole 23, resulting in a silicon layer 13 having a thin portion as shown in arrow A of Fig. 3D and arrow B of Fig. 3E. The resistance of this portion is increased to deteriorate the transistor characteristic. The value of drain current  $I_D$  with respect to a predetermined drain voltage  $V_D$  is decreased as shown in Fig. 4B. There was also a problem that the transistor does not operate due to the fact that there is some portion where silicon layer 13 is completely removed to cut off source region 17 or drain region 18.

#### SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor device improved in transistor characteristic by suppressing decrease of film thickness in the semiconductor layer caused by over-etching, and a method of forming thereof.

A semiconductor device according to the present invention includes a semiconductor layer formed on an insulator layer, a channel region of a first conductivity type formed within the semiconductor layer, additional source/drain regions of a second conductivity type formed within the semiconductor layer adjacent to the sides of the channel region, and a gate electrode formed above the channel region with a dielectric thin film therebetween. A first sidewall spacer is formed at the sidewall of the gate electrode. An etching-resistant metal layer is formed on the surface of the semiconductor layer outside the first sidewall spacer. A second sidewall spacer is formed at the outer surface of the first sidewall spacer. Source/drain regions of a second conductivity type having a concentration higher than that of the additional source/drain regions are formed in the semiconductor layer outside the region of the second sidewall spacer adjacent to the additional source/drain regions.

A method of manufacturing a semiconductor device according to the present invention comprises the steps of forming a dielectric thin film on a semiconductor layer formed on an insulating layer, and forming a gate electrode on this dielectric thin film. Using the gate electrode as a mask, impurities of a second

conductivity type are implanted into the semiconductor layer to form additional source/drain regions. A first sidewall spacer is formed at the left and right sidewalls of the gate electrode, followed by forming an etching-resistant metal layer in self-alignment at the region where the semiconductor layer is exposed excluding the surface of the first sidewall spacer. After the formation of the metal layer, a second sidewall spacer is formed at the outer surface of the first sidewall spacer. Using this second sidewall spacer as a mask, impurities of a second conductivity type are implanted to form source/drain regions having a concentration higher than that of the additional source/drain regions.

A semiconductor device and a method of manufacturing the same according to the present invention has a double layered structure of a first sidewall spacer formed at the sidewall of a gate electrode and a second sidewall spacer formed at the outer surface thereof. The first sidewall spacer is used as a mask for forming a metal layer on the surface of source/drain regions. The second sidewall spacer is used as a mask in the formation of source/drain regions of high concentration in an LDD structure. This allows the formation of the first sidewall spacer with relatively thin thickness in which the maximum width is approximately 1000Å. Therefore, over-etching of the source/drain regions is suppressed to a very low degree in anisotropic etching of forming the first sidewall spacer. The formation of an etching-resistant metal layer on the source/drain regions prevents over-etching of the source/drain regions in anisotropic etching in forming the second sidewall spacer.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWING

Fig. 1A is a sectional view of a conventional bulk type CMOS.

Fig. 1B is a sectional view of a conventional SOI-CMOS.

Fig. 2 is a sectional view of a conventional thin SOI-MOSFET.

Figs. 3A - 3F are sectional views of a conventional SOI-MOSFET showing the manufacturing steps thereof.

Fig. 4A is a graph showing the  $V_D - I_D$  characteristic degraded by the so-called punch through phenomenon in a conventional bulk type MOSFET.

Fig. 4B is a graph of the transistor characteristic where resistance is increased due to a thin silicon layer in source/drain regions in a conventional SOI-MOSFET.

Fig. 5 is a sectional view of a SOI-MOSFET according to an embodiment of the present invention.

Figs. 6A - 6H are sectional views of the SOI-MOSFET of the embodiment showing the manufacturing steps thereof.

Fig. 7 is a sectional view of a structure where a titanium silicide layer is formed on the surface of the source/drain regions of a bulk type MOSFET according to conventional technology associated with the present invention.

Fig. 8 is a sectional view of a CMOS having the SOI structure in which the present invention is applied to.

Fig. 9 is a graph of the  $V_D - I_D$  characteristic of a thin SOI-MOSFET according to the embodiments of the present invention.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will be explained hereinafter with reference to the drawings. Fig. 5 shows a sectional view of a thin film SOI-MOSFET of the present embodiment. Referring to Fig. 5, this thin film SOI-MOSFET has an insulator layer 12 formed on a silicon substrate 11. A thin silicon layer 13 of approximately 300 - 1500Å in thickness is formed as a semiconductor layer on insulator layer 12. Silicon layer 13 has a channel region 14 of low p type impurity concentration (for example  $10^{16} - 10^{17}/\text{cm}^3$ ) formed in the proximity of the center thereof. An additional source region 15 and an additional drain region 16 each having a n type impurity concentration of an intermediate level (for example  $10^{18}/\text{cm}^3$ ) are formed adjacent to the left and right sides of channel region 14. Additional source region 15 and additional drain region 16 have a source region 17 and a drain region 18, respectively, of high n type impurity concentration (for example  $10^{19} - 10^{21}/\text{cm}^3$ ) formed adjacent to the sides of channel region 14. A gate electrode 20 is formed above channel region 14 with a dielectric thin film therebetween.

The above structure is similar to the aforementioned conventional embodiment of Fig. 2. The present embodiment shows a first sidewall spacer 25 of relatively thin thickness where the maximum width is approximately 1000Å at the sidewall of gate electrode 20. A metal layer 27 formed of a thin titanium silicide layer of approximately 500Å in thickness, for example, is formed on the surface of silicon layer 13 which is not covered with gate electrode 20 or first sidewall spacer 25, and on gate electrode 20. A second sidewall spacer 26 having a maximum thickness of approximately 3000Å is formed at the outer surface of first sidewall spacer 25. An additional source region 15 or an additional drain region 16 is provided in silicon layer 13 beneath first sidewall spacer 25. A depression or reduction in film thickness due to over-etching is not seen in second sidewall spacer 26 and in silicon layer 13 at the bottom of contact hole 23.

Because metal layer 27 of low resistance is provided in silicon layer 13 in the structure, it is possible to reduce resistance of source region 17 and drain region 18.

The manufacturing steps of the SOI-MOSFET of the embodiment in Fig. 5 will be explained with reference to Figs. 6A - 6H. According to the method of manufacturing an SOI-MOSFET of the present embodiment, oxygen ions are implanted into silicon substrate 11 at an injection energy of 200KeV and a dosage of  $2 \times 10^{18}/\text{cm}^2$ , followed by a heating process of approximately 1350°C. This forms an insulator layer 12 in silicon substrate 11, leaving a thin silicon layer 13 on the surface thereof. Then, silicon layer 13 is processed in an island-like manner to form an active region (Fig. 6A). A channel region 14 is formed introducing impurities of p type into silicon layer 13. The surface of silicon layer 13 is thermal-oxidized to form a dielectric thin film 19. Then, a gate electrode 20 of polycrystalline silicon is formed (Fig. 6B). Using gate electrode 20 as a mask, n type impurities such as phosphorus ions are implanted at an injection energy of 80KeV and a dosage of  $1 \times 10^{13}/\text{cm}^2$  to form an additional source region 15 and an additional drain region 16 of a concentration of approximately  $10^{18}/\text{cm}^3$  (Fig. 6C).

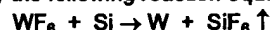
The above described manufacturing steps are similar to those of the aforementioned conventional embodiment. In the present embodiment, a CVD oxide film 25a is formed (Fig. 6D), followed by formation of a first sidewall spacer 25 by reactive ion etching (Fig. 6E). If the film thickness of CVD oxide film 25a is approximately set to 1000Å for example, reduction in thickness of silicon layer 13 due to over-etching is very low. This is because the over-etching amount of CVD oxide film 25a is set to be approximately 200Å which is 20% of 1000Å and the etching selectivity of silicon is approximately 1/5 of CVD oxide film 25a, so that the over-etching amount of silicon layer 13 is approximately 40Å.

A metal layer 27 of titanium silicide, for example, is formed on silicon layer 13 or on gate electrode 20 by a self-aligning method described hereinafter (Fig. 6F). In forming a titanium silicide layer for metal layer 27, titanium is deposited all over the surface to a thickness in a range from several hundreds to a thousand Å (several 100sÅ - 1000Å), followed by heat process to silicide the exposing portion of silicon or polycrystalline silicon, resulting in formation of a titanium silicide layer. Titanium on insulator layer 12 or on the surface of sidewall spacer 25 is left unreacted, or is nitrified to be changed to titanium nitride. By removing the unreacted titanium or titanium nitride with sulfuric acid, metal layer 27 of titanium silicide layer is selectively formed on silicon layer 13 or gate electrode 20. Next, a CVD oxide film of approximately 3000Å thickness is deposited all over the surface to be subjected to anisotropic etching for forming a second sidewall

spacer 26. Using sidewall spacer 26 as a mask, n type impurities such as phosphorus ions and arsenic ions are added to form a source region 17 and a drain region 18 (Fig. 6G). In forming second sidewall spacer 26, over-etching of silicon layer 13 is prevented since metal layer 27 covers silicon layer 13. This is because the etching selectivity of metal layer 27 with respect to the CVD insulating film forming sidewall spacer 26 is decreased to approximately 1/20.

The formation of interconnection layer 24 results in the sectional view of Fig. 6H. Interconnection layer 24 is electrically connected to source region 17 and drain region 18 via metal layer 27 in contact hole 23.

Although titanium silicide is described as the material of metal layer 27 in the present embodiment, similar effects can be obtained using other materials such as cobalt silicide or selective tungsten layer as long as the metal layer has conductivity and etching resistance, and is capable of being formed in self-alignment. Selective tungsten layer takes advantage of the fact that the core of tungsten is easily generated on silicon by the following reaction equation.



Although a monocrystalline silicon layer is used as the semiconductor layer in the present embodiment, similar effects can be obtained using a semiconductor layer of polycrystalline silicon or gallium arsenic.

Although the present embodiment is described in which an n channel MOSFET is employed, a p channel MOSFET may be used. Identical effects can be obtained with only the conductivity type reversed.

Although the present invention is applied to a thin film SOI-MOSFET in the present embodiment, the prevention of over-etching which is the object of the present invention is also effectively applicable to the so-called bulk MOSFET provided on a semiconductor substrate. The present invention has particular effect in a semiconductor device having a relatively shallow source/drain junction.

As a conventional technology associated with the above described embodiment, a structure where a titanium silicide film is formed on the surface of the source/drain regions of a bulk type MOSFET of Fig. 7 is disclosed in Japanese Patent Laying-Open No. 61-270870. Referring to Fig. 7, the structure disclosed in the aforementioned publication has a gate electrode 103 formed above silicon substrate 101 with an insulating film 102 therebetween. At the left and right sides of gate electrode 103, sidewall spacers 105a and 105b of an insulating film are formed which insulates gate electrode 103 from impurity diffusion layers 104a and 104b which become the source/drain regions. A titanium silicide film 106a is formed in impurity diffusion layer 104a. A titanium silicide film 106c is formed on gate electrode 103. A titanium silicide film 106b is formed on impurity diffusion layer 104b. An oxide titanium film 107a is formed in titanium silicide

film 106a, sidewall spacer 105a, and titanium silicide film 106c. An oxide titanium film 107c is formed on titanium silicide film 106b, sidewall spacer 105b, and titanium silicide film 106c. An oxide titanium film 107b is formed on titanium silicide film 106b and on a relatively thick insulating film 108. According to this structure, titanium silicide layers 106a and 106b contribute to reduction in sheet resistance of impurity diffusion layers 104a and 104b.

However, impurity diffusion layers 104a and 104b will be over-etched by the anisotropic etching step in forming sidewall spacers 105a and 105b because sidewall spacers 105a and 105b of Fig. 7 are of a single layer structure relatively great in thickness. The application of such a structure in a semiconductor device having an active region of a thin semiconductor layer, such as a thin type SOI-MOSFET, cannot have the problem solved of increase in resistance of the source/drain regions due to over-etching.

An embodiment where the present invention is applied to a CMOS having an SOI structure will be explained hereinafter. Fig. 8 shows a sectional view of an SOI type CMOS where the present invention is applied to the conventional structure of Fig. 1A. Referring to Fig. 8, silicon layers 113a and 113b as the semiconductor layer are formed in an island-like manner on a silicon substrate 111 with an insulator layer 112 therebetween. An n channel MOS 101 is formed at silicon layer 113a. A p channel MOS 102 is formed at silicon layer 113b. Specifically, a p channel region 114a is formed in the middle of silicon layer 113a. An n type additional source region 115a and an additional drain region 116a are formed adjacent to the left and right sides of channel region 114a. A source region 117a and a drain region 118a are formed adjacent to additional source region 115a and additional drain region 116a, respectively. A gate electrode 120 is formed above channel region 114a with a dielectric thin film 119 therebetween. A first sidewall spacer 125 and a second sidewall spacer 126 forming a double layered structure are formed at the left and right sides of gate electrode 120. A metal layer 127 such as of titanium silicide layer is formed on the surface of silicon layer 113a at the region outside first sidewall spacer 125 and on the surface of gate electrode 120. Silicon layer 113b isolated from silicon layer 113a by a field insulating film 103 has a channel region 114b of the n type formed in the middle thereof. An additional source region 115b and an additional drain region 116b of the p type are formed adjacent to the left and right sides of channel region 114b. A high concentration p type source region 117b and a drain region 118b are formed on the further outer left and right sides of additional source and drain regions of 115b and 116b, respectively. The structures of gate electrode 120 and first sidewall spacer 125, and second sidewall spacer 126 and metal layer 127 are similar to those of the above described n channel MOS 101.

According to an SOI type CMOS having the above described structure is free of soft error and latch up phenomenon. Also, resistance of the source/drain regions are held low to improve the current characteristic of the transistor.

The  $V_D - I_D$  characteristic of the SOI-MOSFET obtained by the above described embodiment is superior as shown in the graph of Fig. 9.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

## Claims

1. A semiconductor device comprising:
  - a semiconductor layer (13, 113a, 113b) formed on an insulator layer (12, 112),
  - a channel region of a first conductivity type (14, 114a, 114b) formed in said semiconductor layer (13, 113a, 113b),
  - additional source/drain regions (15, 16, 115a, 115b, 116a, 116b) of a second conductivity type formed in said semiconductor layer (13, 113a, 113b) adjacent to the left and right sides of said channel region (14, 114a, 114b),
  - a gate electrode (20, 120) formed above said channel region (14, 114a, 114b) with a dielectric thin film (19, 119) therebetween,
  - a first sidewall spacer (25, 125) provided on the left and right sidewalls of said gate electrode (20, 120),
  - a metal layer (27, 127) having etching-resistance formed at the surface of said semiconductor layer (13, 113a, 113b) in a region outside the region where said first sidewall spacer (25, 125) is formed,
  - a second sidewall spacer (26, 126) provided to cover the outer surface of said first sidewall spacer (25, 125), and
  - source/drain regions (17, 18, 117a, 117b, 118a, 118b) having a concentration higher than that of said additional source/drain regions (15, 16, 115a, 115b, 116a, 116b), and formed in said semiconductor layer (13, 113a, 113b) in a region outside the region where said second sidewall spacer (26, 126) is formed.
2. The semiconductor device according to claim 1, wherein said semiconductor layer (13, 113a, 113b) comprises a silicon layer of 300 - 1500Å in thickness.
3. The semiconductor device according to claim 1, wherein said metal layer (27, 127) comprises a

titanium silicide layer.

4. The semiconductor device according to claim 1, wherein

said channel region (14, 114a, 114b) has a p type impurity concentration of  $10^{16} - 10^{17}/\text{cm}^3$ ,  
said additional source/drain regions (15, 16, 115a, 115b, 116a, 116b) have an n type impurity concentration of approximately  $10^{18}/\text{cm}^3$ ,  
said source/drain regions (17, 18, 117a, 117b, 118a, 118b) have an n type impurity concentration of  $10^{19} - 10^{21}/\text{cm}^3$ .

5. The semiconductor device according to claim 1, wherein said first sidewall spacer (25, 125) is formed thinner than said second sidewall spacer (26, 126).

6. The semiconductor device according to claim 5, wherein

said first sidewall spacer (25, 125) has a maximum thickness of approximately 1000Å,  
said second sidewall spacer (26, 126) has a maximum thickness of approximately 3000Å.

7. The semiconductor device according to claim 3, wherein said metal layer (27, 127) comprises a titanium silicide layer of approximately 500Å in thickness.

8. A semiconductor device comprising:

two semiconductor layers (113a, 113b) formed on a same insulator layer (112) insulation-isolated from each other,

a gate electrode (120) formed above each of said semiconductor layers (113a, 113b) with a gate dielectric thin film (119) therebetween,

a first sidewall spacer (125) provided at the left and right sidewalls of each said gate electrode (120),

a metal layer (127) having etching-resistance, and formed in a region outside the region where said sidewall spacer (25, 125) is formed at the surface of said each semiconductor layer (113a, 113b), and

a second sidewall spacer (126) formed to cover the outer surface of said each sidewall spacer (125),

wherein one of said semiconductor layer (113a) of said two semiconductor layers (113a, 113b) comprises

a channel region (114a) of p type right beneath said gate electrode (120),

additional source/drain regions (115a, 116a) of n type formed adjacent to the left and right sides of said channel region (114a), and

source/drain regions (117a, 118a) of n type having a concentration higher than that of

said additional source/drain regions (115a, 116a), and formed adjacent to said additional source/drain regions (115a, 116a) at a region outside the region where said second sidewall spacer (126) is formed,

wherein the other semiconductor layer (113b) comprises

a channel region (114b) of n type right beneath said gate electrode (120),

additional source/drain regions (115b, 116b) of p type formed adjacent to the left and right sides of said channel region (114b), and

source/drain regions (117b, 118b) of p type having a concentration higher than that of said additional source/drain regions (115b, 116b), and formed adjacent to said additional source/drain regions (115b, 116b) in a region outside the region where said second sidewall spacer (126) is formed.

9. The semiconductor device according to claim 8, wherein said semiconductor layer (113a, 113b) comprises a silicon layer of 300 - 1500Å in thickness.

10. The semiconductor device according to claim 8, wherein said metal layer (127) comprises titanium silicide.

11. The semiconductor device according to claim 8, wherein

said each channel region (114a, 114b) has an impurity concentration of  $10^{16} - 10^{17}/\text{cm}^3$ ,

said additional source/drain regions (115a, 115b, 116a, 116b) have an impurity concentration of approximately  $10^{18}/\text{cm}^3$ , and

said source/drain regions (117a, 117b, 118a, 118b) have an impurity concentration of  $10^{19} - 10^{21}/\text{cm}^3$ .

12. The semiconductor device according to claim 8, wherein said first sidewall spacer (125) is formed thinner than said second sidewall spacer (126).

13. The semiconductor device according to claim 12, wherein

said first sidewall spacer (125) comprises a maximum thickness of approximately 1000Å and,

said second sidewall spacer (127) comprises a maximum thickness of approximately 3000Å.

14. The semiconductor device according to claim 10, wherein said metal layer (127) comprises a titanium silicide layer of approximately 500Å in thickness.

15. A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor layer (13, 113a, 113b) of a first conductivity type on an insulator layer (12, 112),

forming a dielectric thin film (19, 119) on said semiconductor layer (13, 113a, 113b),

forming a gate electrode (20, 120) on said dielectric thin film (19, 119),

forming additional source/drain regions (15, 16, 115a, 115b, 116a, 116b) by implanting impurities of a second conductivity type into said semiconductor layer (13, 113a, 113b) using said gate electrode (12, 120) as a mask,

forming a first sidewall spacer (25, 125) on the left and right sidewalls of said gate electrode (20, 120),

forming a metal layer (27, 127) in self-alignment having etching-resistance at the region where said semiconductor layer (13, 113a, 113b) is exposed and on said gate electrode (20, 120), excluding the surface of said first sidewall spacer (25, 125).

16. The method of manufacturing a semiconductor device according to claim 15, wherein said step of forming a semiconductor layer (13, 113a, 113b) of the first conductivity type on said insulator layer (12, 112) comprises the steps of

implanting oxygen ions into a silicon substrate (11, 111) at a predetermined injection energy and a predetermined dosage, followed by a heating process, leaving a silicon layer (13, 113a, 113b) of a predetermined depth from the surface of said silicon substrate (11, 111) to form an insulator layer (12, 112) of SiO<sub>2</sub> within said silicon substrate (11, 111),

implanting impurities of the first conductivity type into said silicon layer (13, 113a, 113b) on said insulator layer (12, 112).

17. The method of manufacturing a semiconductor device according to claim 15, wherein said step of forming said metal layer (27, 127) comprises the step of

depositing titanium all over the surface to a thickness of several 100sÅ - 1000Å, followed by a heating process to silicide the same to remove unreacted titanium.

18. The method of manufacturing a semiconductor device according to claim 15, further comprising the steps of:

forming a second sidewall spacer (26, 126) to cover the outer surface of said first sidewall spacer (25, 125) after the step of forming said metal layer (27, 127), and

forming source/drain regions (17, 18,

117a, 117b, 118a, 118b) having a concentration higher than that of said additional source/drain regions (15, 16, 115a, 115b, 116a, 116b), by implanting impurities of second conductivity type into said semiconductor layer (13, 113a, 113b) using said second sidewall spacer (26, 126) and said gate electrode (20, 120) as masks.

19. The method of manufacturing a semiconductor device according to claim 18, wherein said step of forming said first sidewall spacer (25, 125) further comprises the steps of forming a CVD oxide film (25a) to a thickness of approximately 1000Å, and applying reactive ion etching to said CVD oxide film (25a),

wherein said step of forming said second sidewall spacer (26, 126) comprise the steps of forming a CVD oxide film of a thickness of approximately 3000Å, and applying reactive ion etching to said CVD oxide film.

20. The method of manufacturing a semiconductor device according to claim 15, wherein said step of forming said metal layer (27, 127) comprises the step of forming a WF<sub>6</sub> film, followed by reaction of the same with a layer including silicon to generate a core of tungsten for forming a selected tungsten layer.

21. A semiconductor device comprising:

a semiconductor layer (13, 113a, 113b) formed on an insulator layer (12, 112),

a channel region of a first conductivity type (14, 114a, 114b) formed in said semiconductor layer (13, 113a, 113b),

source/drain regions (15, 16, 17, 18, 115a, 115b, 116a, 116b, 117a, 117b, 118a, 118b) of a second conductivity type formed in said semiconductor layer (13, 113a, 113b) adjacent to the left and right sides of said channel region (14, 114a, 114b),

a gate electrode (20, 120) formed above said channel region (14, 114a, 114b) with a dielectric thin film (19, 119) therebetween,

a sidewall spacer (25, 125) provided on the left and right sidewalls of said gate electrode (20, 120),

a metal layer (27, 127) having etching-resistance formed at the surface of said semiconductor layer (13, 113a, 113b) in a region outside the region where said sidewall spacer (25, 125) is formed.



FIG. 1A

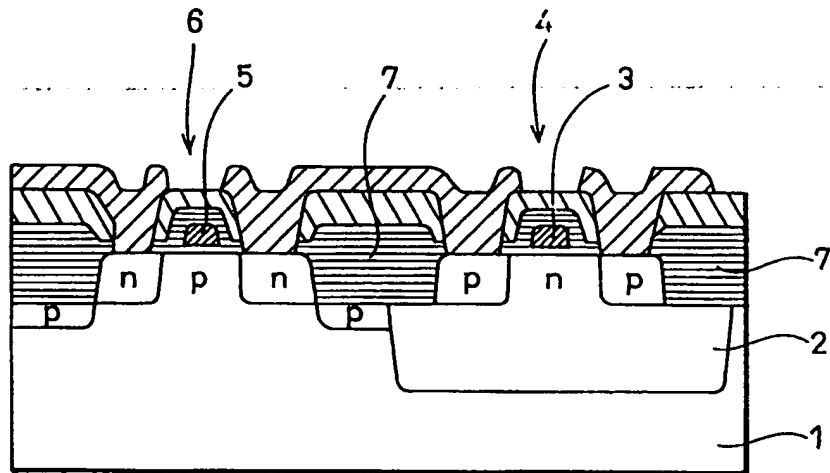


FIG. 1B

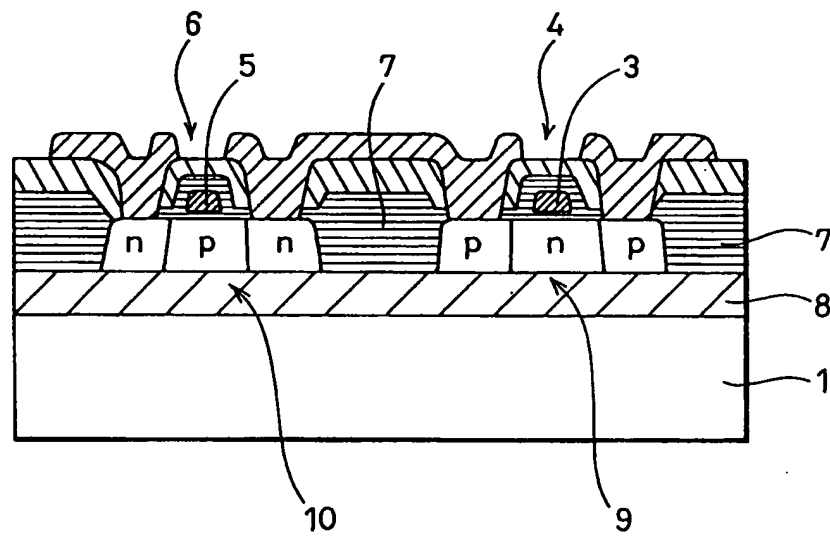


FIG. 2

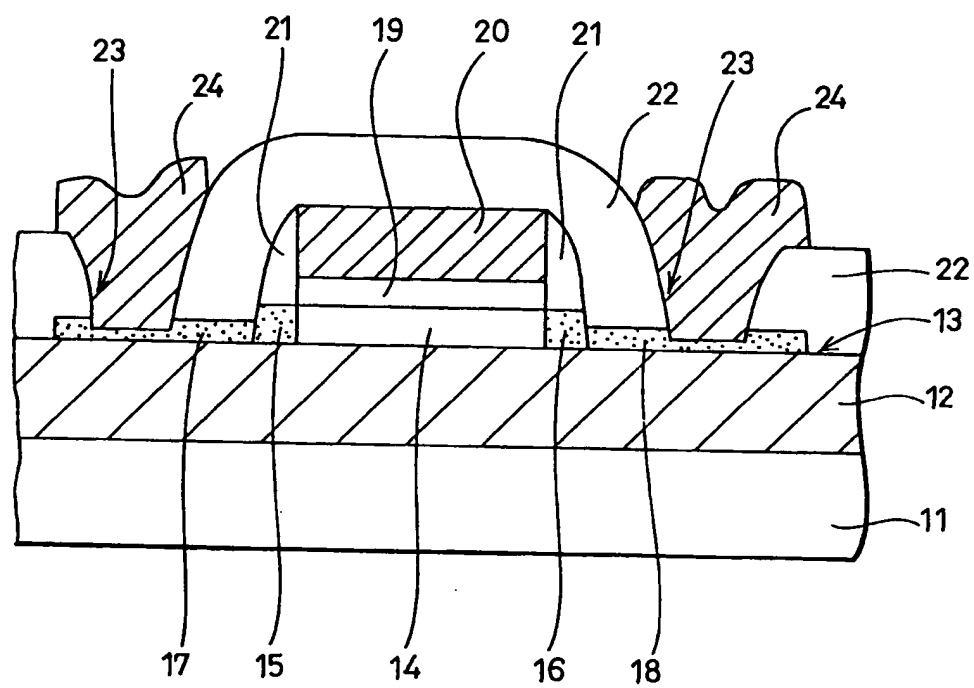


FIG. 3A

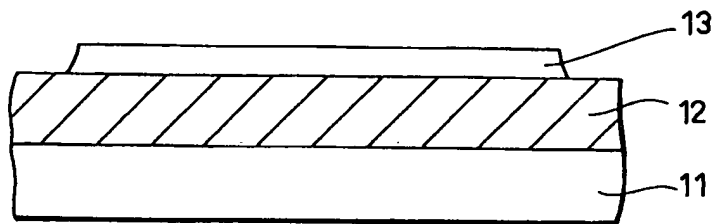


FIG. 3B

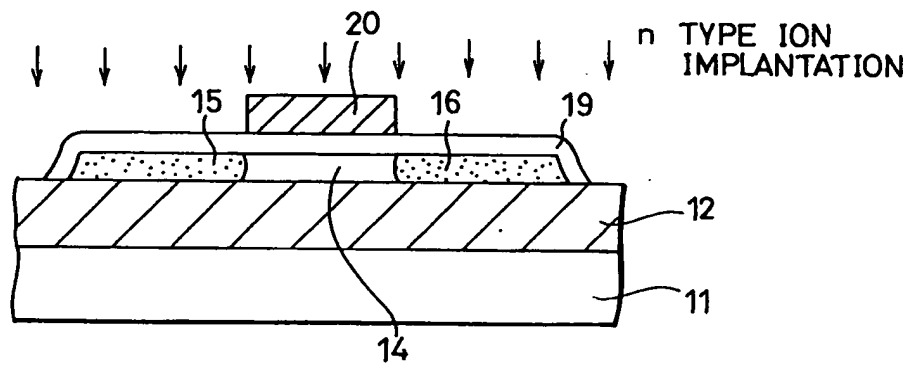


FIG. 3C

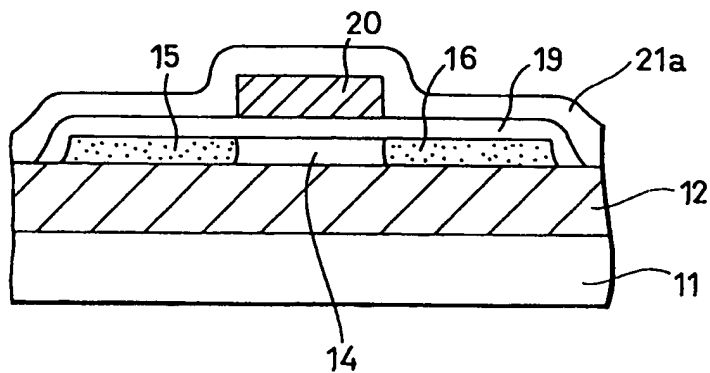


FIG. 3D

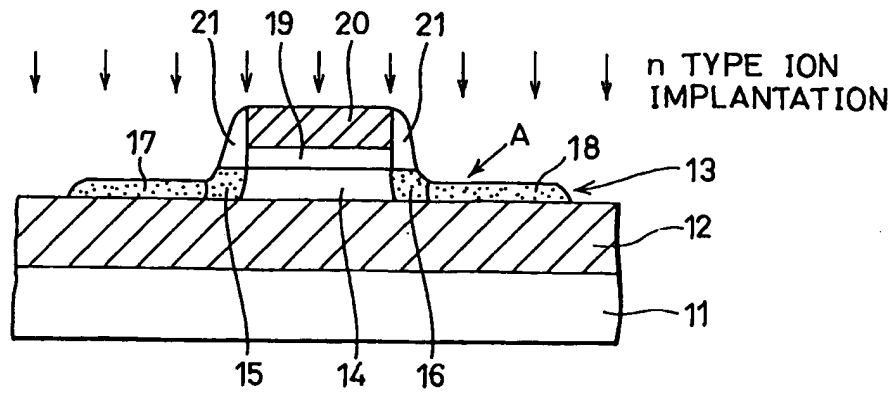


FIG. 3E

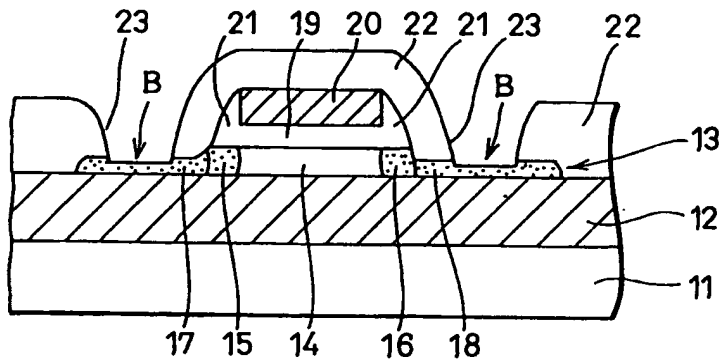


FIG. 3F

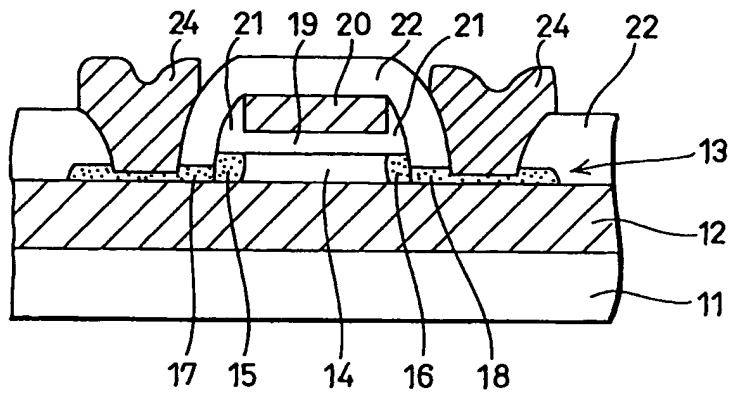


FIG.4A

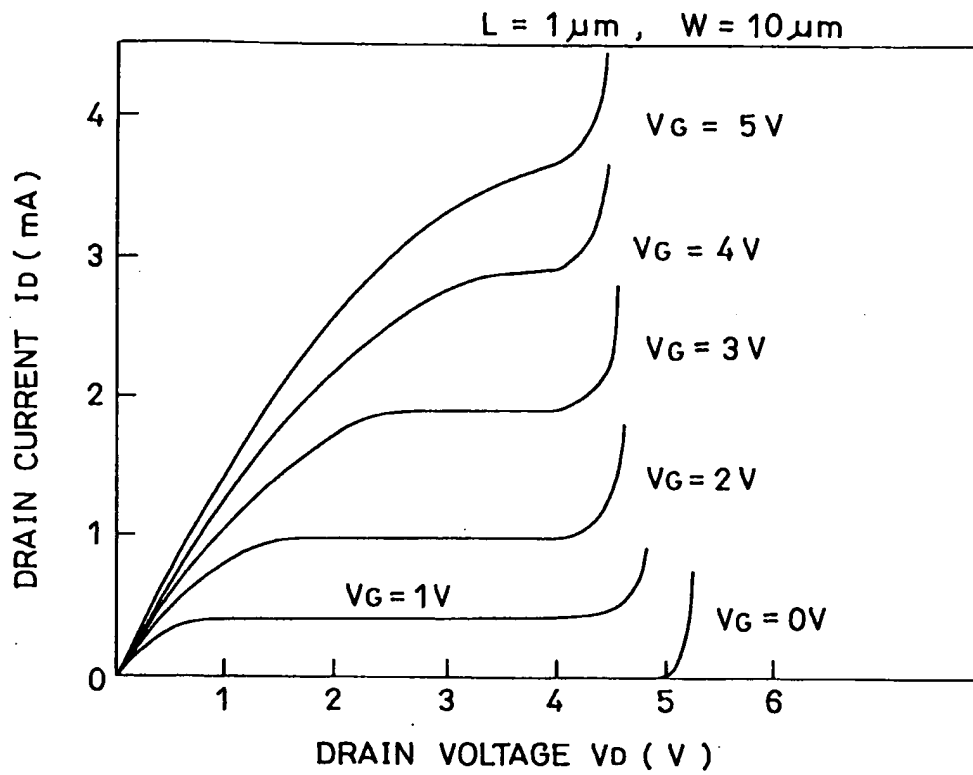


FIG.4B

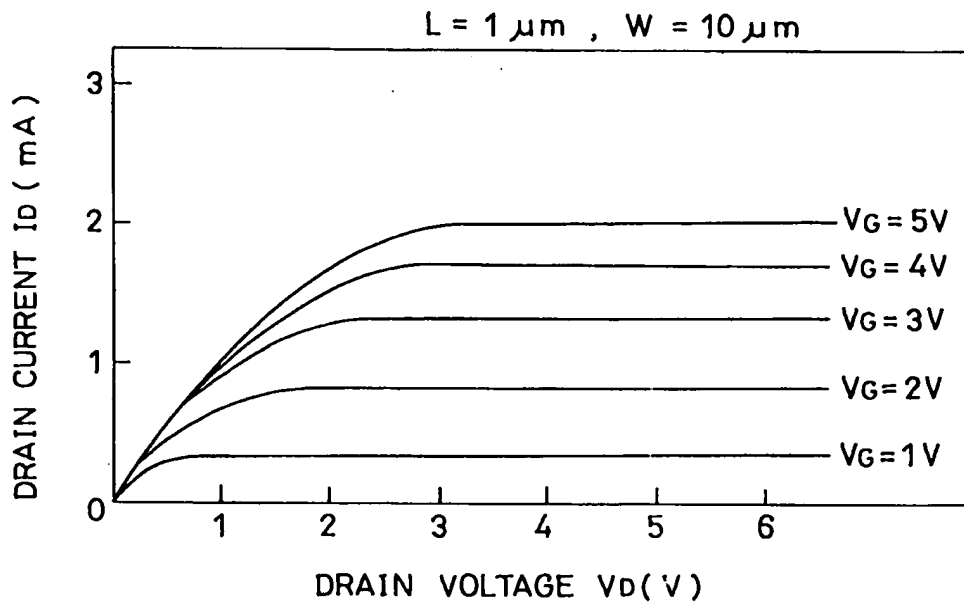


FIG. 5

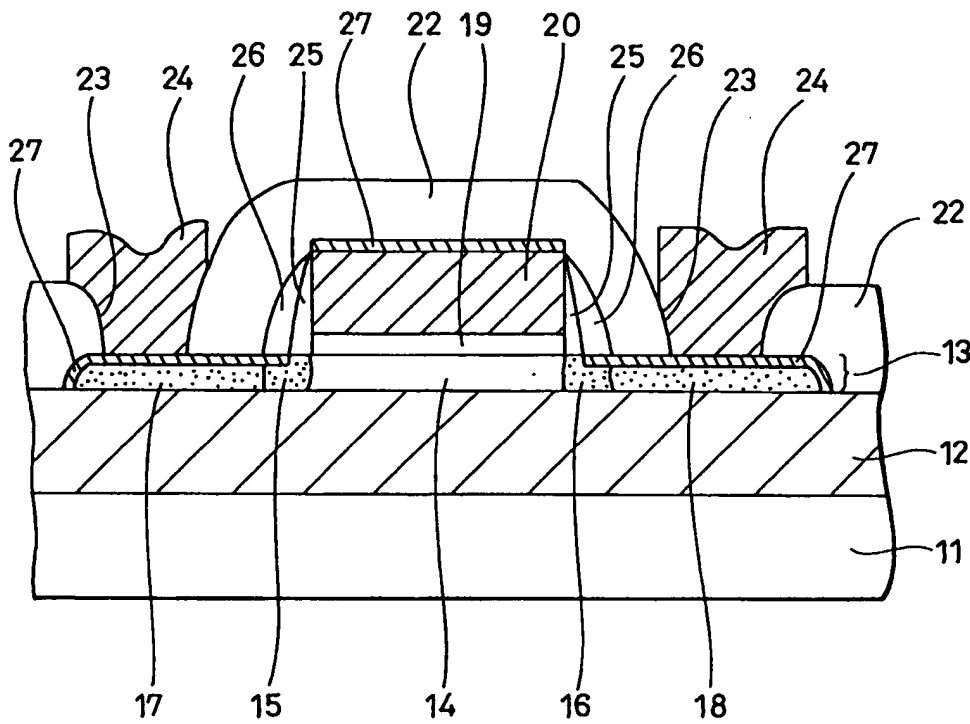


FIG. 6A

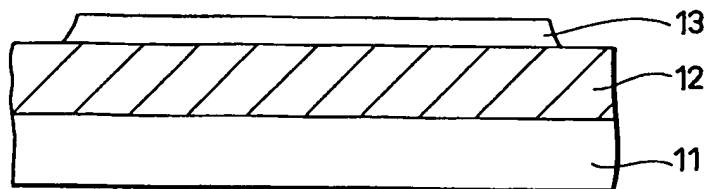


FIG. 6B

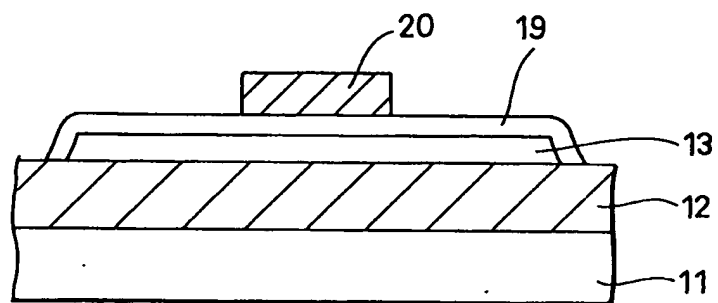


FIG. 6C

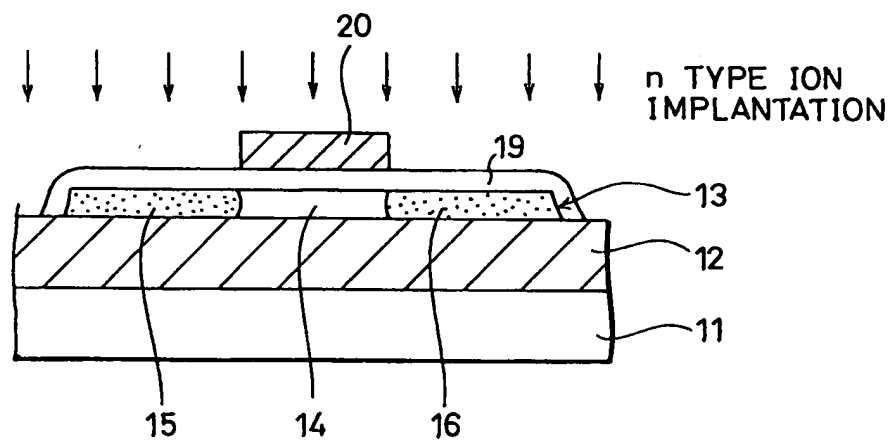


FIG. 6D

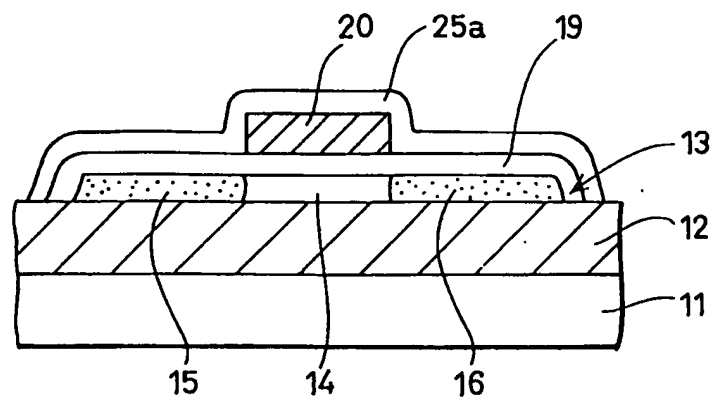


FIG. 6E

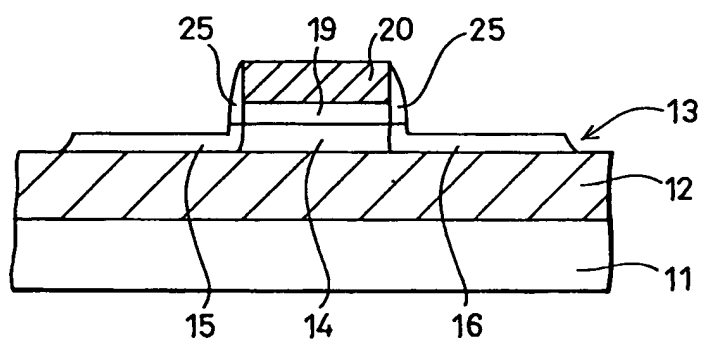


FIG. 6F

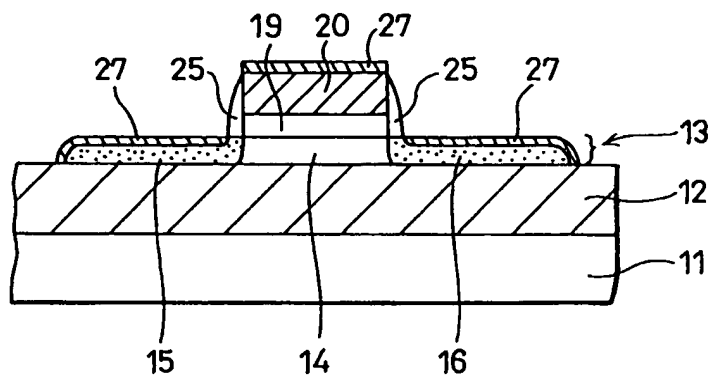




FIG. 6G

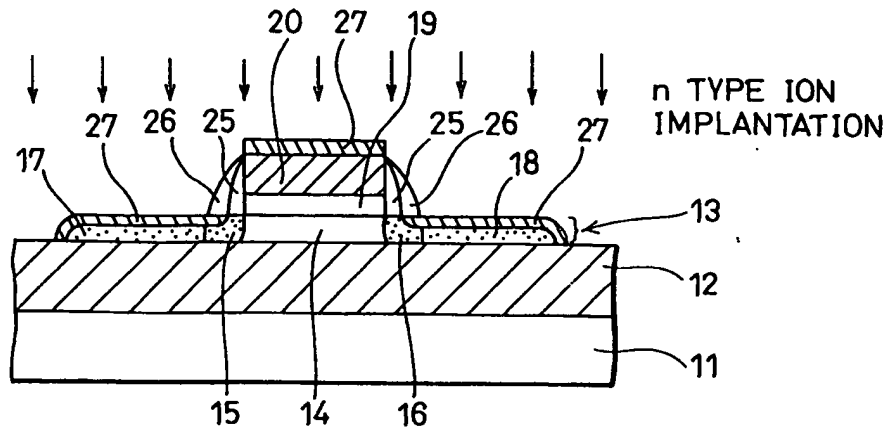


FIG. 6H

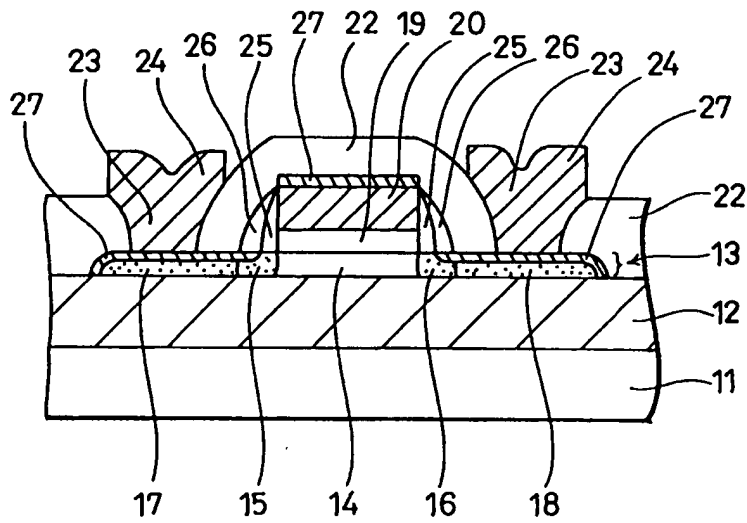


FIG. 7

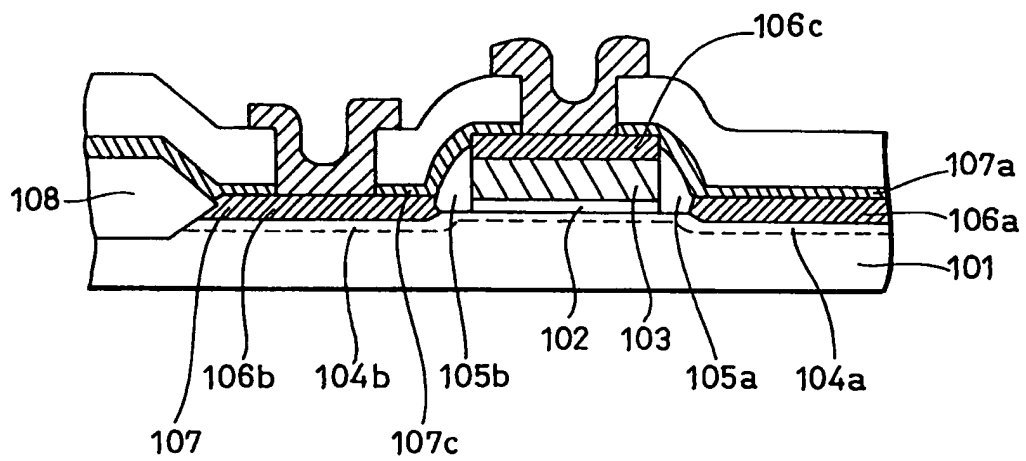


FIG. 8

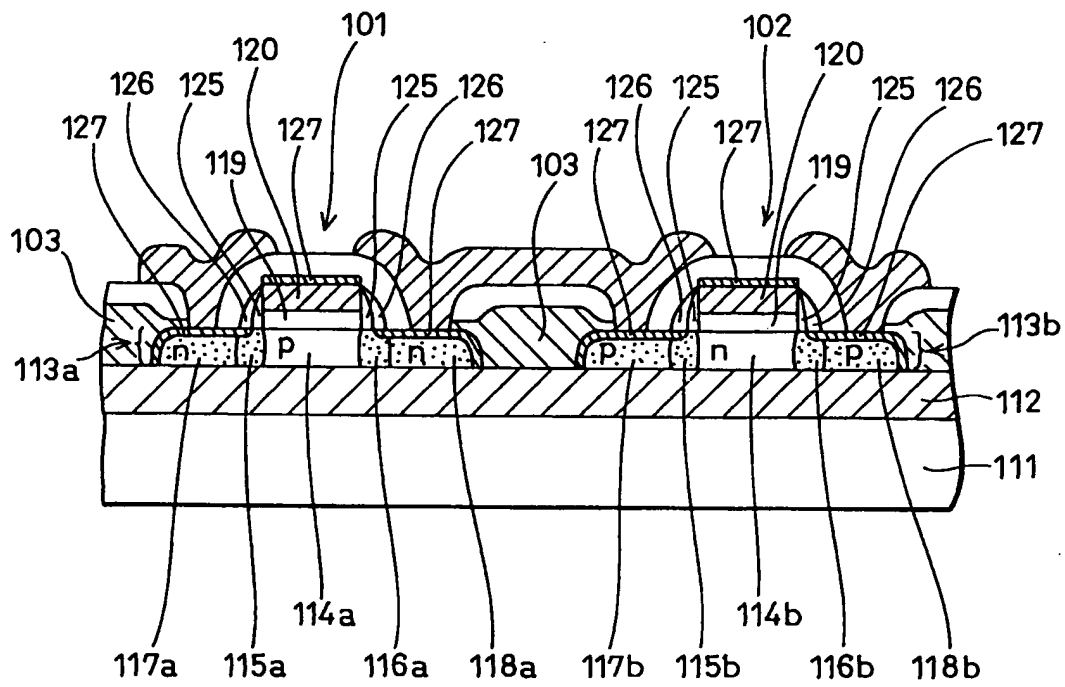
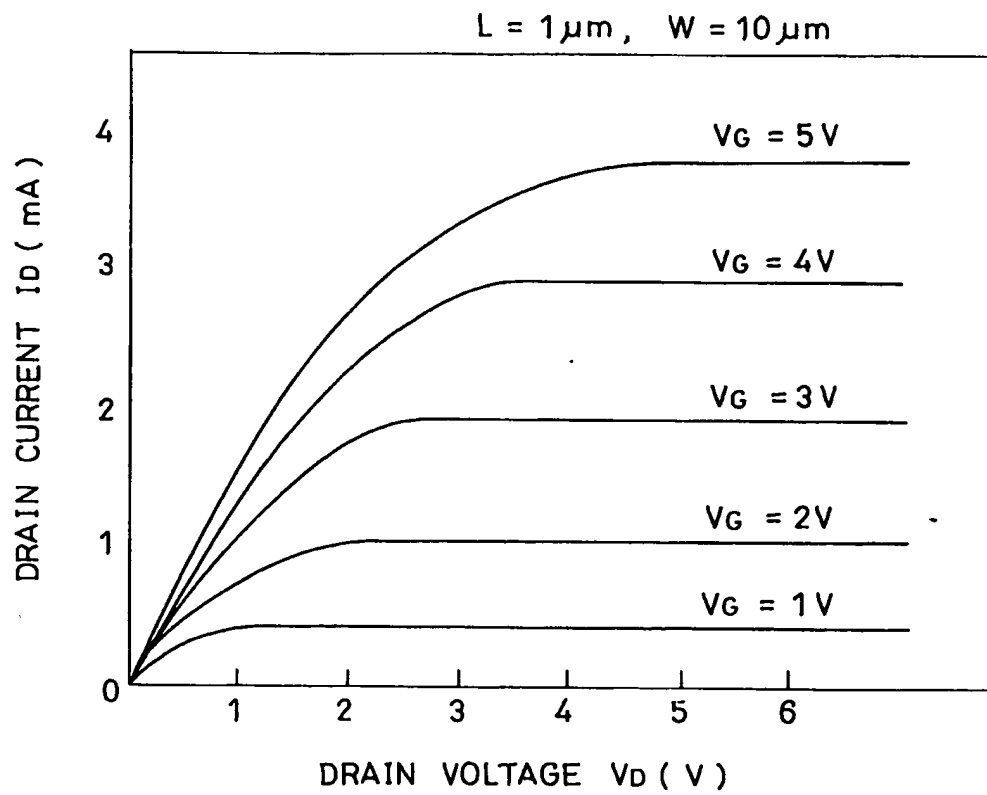


FIG.9





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## EUROPEAN SEARCH REPORT

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	PATENT ABSTRACTS OF JAPAN vol. 11, no. 376 (E-563)8 December 1987 & JP-A-62 143 473 ( HITACHI LTD ) 26 June 1987 * abstract *	1,15,17,21	H01L29/784 H01L29/08
Y	PATENT ABSTRACTS OF JAPAN vol. 012, no. 217 (E-624)21 June 1988 & JP-A-63 012 168 ( OKI ELECTRIC IND CO LTD ) 19 January 1988 * abstract *	1	
Y	PATENT ABSTRACTS OF JAPAN vol. 11, no. 212 (E-522)9 July 1987 & JP-A-62 032 653 ( NIPPON TELEGR & TELEPH CORP <NTT> ) 12 February 1987 * abstract *	15,17,21	
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 455 (E-985)28 September 1990 & JP-A-02 181 934 ( MITSUBISHI ELECTRIC CORP ) 16 July 1990 * abstract *	1-7, 15-19	
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 320 (E-651)30 August 1988 & JP-A-63 084 064 ( SEIKO EPSON CORP ) 14 April 1988 * abstract *	3,10,17,20	H01L
D,, A	PATENT ABSTRACTS OF JAPAN vol. 011, no. 127 (E-501)21 April 1987 & JP-A-61 270 870 ( MITSUBISHI ELECTRIC CORP ) 1 December 1986 * abstract *	1-7	
A	PATENT ABSTRACTS OF JAPAN vol. 010, no. 332 (E-453)12 November 1986 & JP-A-61 137 367 ( HITACHI LTD ) 25 June 1986 * abstract *	1-7	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 30 DECEMBER 1991	Examiner MIMOUN B.J.
<p><b>CATEGORY OF CITED DOCUMENTS</b></p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application I : document cited for other reasons A : member of the same patent family, corresponding document</p>			

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	PATENT ABSTRACTS OF JAPAN vol. 010, no. 027 (E-378)4 February 1986 & JP-A-60 186 053 ( SUMA SEIKOSHA KK ) 21 September 1985  -----	8	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 30 DECEMBER 1991	Examiner MINOUN B.J.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document  T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application I : document cited for other reasons ..... & : member of the same patent family, corresponding document			

EPO FORM 1533 (01.82) (P0401)